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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

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EXAMINER	
VERBRUGGE, KEVIN	
ART UNIT	**PAPER NUMBER**
2188	14

DATE MAILED: 04/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,361	WOO ET AL.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,24-26,28-35,38-40 and 52-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,24-26,28-35,38-40 and 52-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/29/04 has been entered.

Response to Amendment

This non-final Office action is in response to Amendment D, paper #13, filed 3/29/04 by fax which canceled claims 22 and 23, amended claims 1, 2, 5, 11, 12, 15, 19, 20, 25, 32, 38, and 52 and added new claims 54-59. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-12, and 14-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa, in view of the Micron Memory Data Book, pp. 1-77 to 1-80, hereinafter simply Micron.

Regarding claims 1 and 11, Ohsawa discloses the claimed plurality of dynamically refreshable memory cells as the DRAM cell array in Figs. 4 and 5.

He shows the claimed dynamically changeable use registers corresponding to groups of memory cells as refresh flags, shown in Figs. 4 and 5.

His memory device is configured to omit refreshing of memory cells that are not in use, as claimed, as indicated by the refresh flags.

Ohsawa does not show the claimed self-refresh logic in the same device as the memory cells to refresh the memory cells.

Micron discloses, on pp. 1-77 through 1-80, a DRAM chip having the claimed self-refresh logic. On page 1-77, in the Features section, Micron teaches that self-refresh is "for low-power data retention". Micron shows the claimed self-refresh logic on page 1-78 as the refresh controller and refresh counter. On page 1-80, first full paragraph, Micron teaches that the self-refresh mode is a "fully static, low-power data retention mode.

In section 4.3, last paragraph, Ohsawa mentions static mode which is the same static self-refresh mode mentioned by Micron. Ohsawa teaches that in the static mode,

DRAM is "only keeping memory by performing refreshes" because the processor is occupied with "I/O, interruptions, and so on."

In summary, Ohsawa mentions that it was known that DRAM devices have a static or self-refresh mode where the devices essentially enter a minimum power consumption state while maintaining their data by refreshing it. Ohsawa does not show the claimed refresh logic for performing these refreshes. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include self-refresh logic such as that shown by Micron in the DRAM devices shown by Ohsawa to perform the self-refreshing of a chip to maintain its data while in the static or self-refresh mode since Ohsawa mentions static mode and since self-refresh was a common feature at the time of the invention. The skilled artisan reading Ohsawa's disclosure would have been motivated to include self-refresh logic on Ohsawa's devices because Ohsawa mentions static mode (self-refresh mode) and because doing so would enable even more power savings than that achievable by Ohsawa's shown devices.

Regarding claims 2, 12, and 16, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the self-refresh logic on the memory devices to not refresh the indicated unused memory cells to minimize power consumption.

Regarding claims 4 and 14, Ohsawa does not show the claimed memory controller, however it is clearly present in his device since he mentions it in section 3.1,

third paragraph, first sentence and since it performs the claimed function of setting the use registers to indicate whether the memory cells are unused.

Regarding claims 5 and 15, Ohsawa's memory controller is apparently implemented on a different device than his use registers since it is not shown in his figures.

Regarding claims 6 and 17, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claim 7, Ohsawa's refresh flags correspond to a set of memory cells as claimed.

Regarding claims 8 and 18, Ohsawa's refresh flags refer to a row of memory cells as claimed.

Regarding claim 9, Ohsawa's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use refresh flags for a bank since this would allow an entire bank to be shut down if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claim 10, a page of memory cells is the same as a row of memory cells.

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Claims 3, 13, 19, 20, 21, 24-26, 28-35, 38-40, and 52-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa in view of the Micron Memory Data Book, pp. 1-77 to 1-80, hereinafter simply Micron, further in view of U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer.

Regarding claims 3, 13, 19, 25, 32, 33, 35, 38, 39, 52, 53, 56, 57, 58, and 59, Ohsawa does not disclose the claimed recent access flags or keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle.

Boyer discloses the recent access flags and keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle (by being read or written).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Boyer's recent access flags in Ohsawa's device to further reduce the number of refresh cycles required to maintain data because Boyer's device is directed to the same goal of reducing the number of refreshes required,

thereby reducing power consumption and enhancing processing speed by improving bandwidth.

Ohsawa does not show the claimed self-refresh logic in the same device as the memory cells to refresh the memory cells.

Micron discloses, on pp. 1-77 through 1-80, a DRAM chip having the claimed self-refresh logic. On page 1-77, in the Features section, Micron teaches that self-refresh is "for low-power data retention". Micron shows the claimed self-refresh logic on page 1-78 as the refresh controller and refresh counter. On page 1-80, first full paragraph, Micron teaches that the self-refresh mode is a "fully static, low-power data retention mode.

In section 4.3, last paragraph, Ohsawa mentions static mode which is the same static self-refresh mode mentioned by Micron. Ohsawa teaches that in the static mode, DRAM is "only keeping memory by performing refreshes" because the processor is occupied with "I/O, interruptions, and so on."

In summary, Ohsawa mentions that it was known that DRAM devices have a static or self-refresh mode where the devices essentially enter a minimum power consumption state while maintaining their data by refreshing it. Ohsawa does not show the claimed refresh logic for performing these refreshes. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include self-refresh logic such as that shown by Micron in the DRAM devices shown by Ohsawa to perform the self-refreshing of a chip to maintain its data while in the static or self-refresh mode since Ohsawa mentions static mode and since self-refresh was a common feature at

the time of the invention. The skilled artisan reading Ohsawa's disclosure would have been motivated to include self-refresh logic on Ohsawa's devices because Ohsawa mentions static mode (self-refresh mode) and because doing so would enable even more power savings than that achievable by Ohsawa's shown devices.

Regarding claims 20 and 54, Ohsawa's use registers are implemented on a different device than his memory controller since the memory controller is not shown in his figures.

Regarding claims 21, 34, and 40, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claim 24, Ohsawa's refresh flags refer to rows as claimed.

Regarding claim 26, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the self-refresh logic on the memory devices to not refresh the indicated unused memory cells to minimize power consumption.

Regarding claim 28, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claim 29, Ohsawa's refresh flags refer to a row of memory cells as claimed.

Regarding claim 30, Ohsawa shows that his use registers are in the memory devices, however, It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

Regarding claim 31, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

Regarding claim 55, Ohsawa's memory cells are implemented on a different device than the memory controller since the memory controller is not shown in his figures.

Conclusion

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents,

Washington, D.C. 20231, faxed to (703) 872-9306, or delivered to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor Receptionist.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

Kevin Verbrugge
Primary Examiner
4/28/04